DECLARATION OF INVENTOR PRASHANT G. KARANDIKAR

I, Prashant G. Karandikar, declare and say as follows:

That I am an inventor named on U.S. Patent Application Serial No. 10/663,359, entitled "Low CTE Metal-Ceramic Composite Articles, and Methods for Making Same", hereinafter referred to as "the '359 Application";

That the above-identified patent application is subject to an obligation of assignment to M Cubed Technologies, Inc., a Delaware corporation with facilities in Monroe, Connecticut and Newark, Delaware;

That I am employed by M Cubed Technologies, Inc. at its Delaware facility as the Director of Research & Development;

That I am named on eight other U.S. Patents or U.S. Patent Applications that are assigned or subject to assignment to M Cubed Technologies, Inc.;

That I am familiar with the invention claimed in the above-identified '359 Patent Application;

That the claimed invention relates to low thermal expansion metal-ceramic composite articles, and particularly to reflector articles such as mirrors;

That the claimed mirror comprises a reflecting surface comprising silicon metal bonded to a substrate;

That the normal form of silicon metal is the crystalline form, and specifically, in polycrystalline form, meaning that a bulk body is made up of small crystals, generally having no particular orientation with respect to one another;

That, with special processing, silicon can be made in other than a polycrystalline form, namely, in a single-crystal form, or in a substantially amorphous form;

That "crystalline" means that the atoms making up the crystal are arranged in very specific locations, specifically in three-dimensional patterns of atoms, thereby forming an array of atoms having long-range order;

That one technique for producing single-crystal silicon is the Czochralski Process, whereby a single crystal of silicon is pulled continuously from a silicon melt using a small rotating single "seed" crystal;

That "amorphous" means that the atoms are not arranged in very specific locations and thus do not form arrays having long-range order;

That "amorphous" in the context of silicon means that the silicon atoms are arranged having only short-range order, meaning that the locations of specific silicon atoms are known only for a short distance beyond any given silicon atom, for example, for those atoms that are immediately adjacent a given atom (the coordination polyhedron);

That one technique for making silicon in substantially amorphous form is to apply the silicon as a coating from a vapor phase such as plasma-enhanced chemical vapor deposition;

That, in one aspect of the invention, namely the invention of independent claim 1 of the application, the reflecting surface comprises silicon metal in substantially amorphous form;

That the induced stress created by the joining of two dissimilar materials is proportional to their difference in CTE and to the temperature change from that at which they were joined,

$$\sigma \text{ proportional to } \Delta\alpha\Delta T$$

where σ denotes stress,
Δ denotes change or "delta",
α denotes coefficient of thermal expansion, and
T denotes temperature;

That Papenburg discloses a substrate having a CTE of about 2.0 ppm/K;

That the CTE of silicon is about 2.3 ppm/K, and thus $\Delta\alpha$ is about 0.3 ppm/K;

That, as a consequence, a stress will be generated between a silicon coating and the substrate of Papenburg, and that such stress will increase in proportion to the joining temperature;

That Papenburg attaches his silicon wafer to his substrate by a brazing process conducted in a temperature range of about 300-600°C;

That if Papenburg were to use a substrate such as mine having a very low CTE of about 1 ppm/K (and so $\Delta\alpha$ is about 1.3 ppm/K), but leave his bonding temperature unchanged, he would increase stress more than four-fold;

That in particular if Papenburg were to do this, he would fracture his silicon reflecting coating;

That I have done this experimental run, among other silicon attachment attempts (runs), and the photos showing a fractured silicon coating are shown in the Appendix;

That consequently, I selected a silicon deposition process that operates at a much lower temperature than the brazing process of Papenburg;

That in particular, I selected a plasma-enhanced chemical vapor deposition (PECVD) process operating at about 100C or less to deposit my silicon reflecting surface;

That the silicon deposited by such a process is at least substantially amorphous;

That my deposited silicon reflecting surface did not crack upon cooling from the deposition temperature, despite my very low substrate CTE of about 1 ppm/K, as indicated by the attached photograph;

That silicon has approximately the same CTE substantially independent of the form that it is in, but if anything, the amorphous form might be expected to have a slightly higher CTE than the crystalline forms, single-crystal and polycrystalline;

That I concluded from this experiment that brazing of crystalline silicon is a satisfactory process when substrate CTE is higher than what I have disclosed, and specifically when substrate CTE is about 2.0 ppm/K, or slightly higher;

That I have furthermore concluded that a silicon attachment or silicon deposition process must be conducted at processing temperatures even lower than brazing temperatures when the substrate CTE is at or below about 1.75 ppm/K, and especially when the substrate CTE is at or below about 1.06 ppm/K;

That the substantially amorphous form of silicon is an inherent characteristic of the silicon deposited by my chosen low-temperature process of PECVD;

That another advantage of a substantially amorphous silicon reflecting surface over polycrystalline silicon is that the substantially amorphous silicon coating can be polished to a better finish (e.g., lower surface roughness) than can a polycrystalline silicon coating; and

That I understand that all statements made herein of my own knowledge are true and that statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Further, declarant sayeth not.

P Karandikar.
Prashant G. Karandikar

11/13/06
Date

Encl.: Appendix describing and summarizing experimental runs

Appendix

Description and summary of experimental runs in support of the Declaration

The following description, photographs and Table form an inherent part of the November 2006 Karandikar Declaration.

This experiment describes a number of candidate attachment schemes for forming a silicon-containing reflecting surface on a lightweight, rigid, low CTE substrate. Unless noted otherwise, the substrate is a composite of carbon fiber reinforcing silicon and silicon carbide. Some additional carbon not in the form of fibers is also present. This composite material substrate has a coefficient of thermal expansion (CTE) of about 1.0 ppm/K. Runs 1, 3, 4 and 5 are actual results; Run 2 is prophetic.

In Run #1, a silicon/silicon carbide (Si/SiC) composite material made by a reaction-bonding process (e.g., infiltration of molten silicon) and having a CTE similar to that of silicon (about 2.9 ppm/K) was contacted to the substrate and heated to a temperature of about 1424°C in vacuum. Residual silicon metal in both composite and substrate melts and flows together, thereby joining the two bodies. The difference in CTE ("CTE mismatch") between the Si/SiC composite surface and the substrate generated enough stress in cooling to ambient from the processing temperature of about 1425°C (silicon melt temperature) that cracking of the Si/SiC composite in multiple locations resulted.

In Run #2, elemental silicon metal is applied by a chemical vapor deposition process instead of by reaction-bonding. The process temperature is about 1300°C. The silicon layer applied to the substrate cracks.

In Run #3, a single crystal silicon wafer was brazed to the substrate using a brazing alloy consisting of 10 wt% aluminum, balance silicon. The process temperature was about 600°C. The silicon wafer still cracked. Macroscopic and microphotographs are shown in Figures 1 and 2 below.

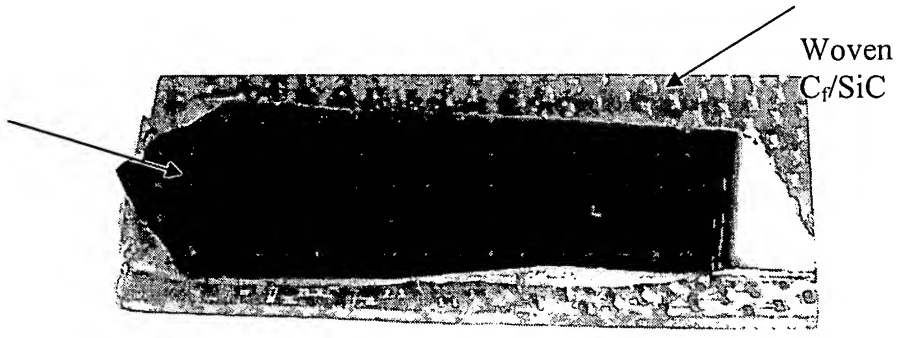

Figure 1. A front (silicon on top) view of specimen in Run #3 (silicon-to-woven C_f/SiC brazed joint). The woven C_f/SiC composite substrate is observable in some areas not covered by the silicon.

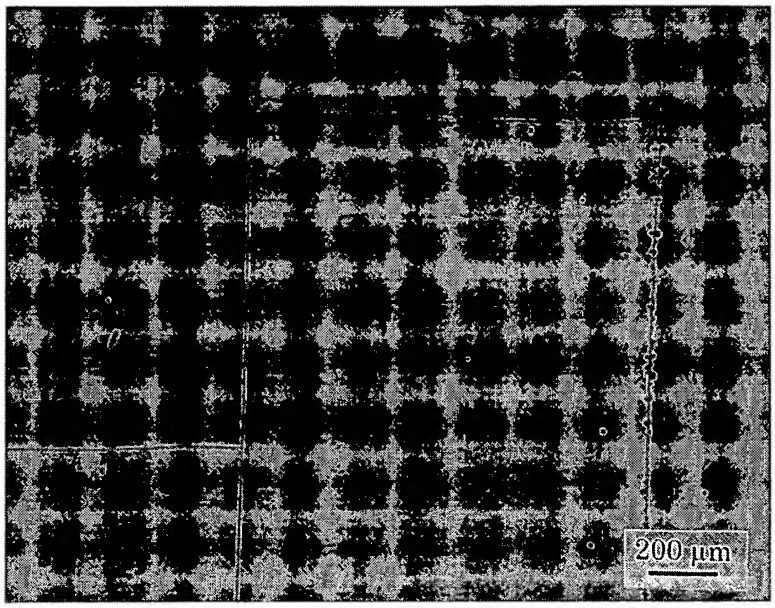

Figure 2. A micrograph of the surface of silicon wafer brazed to woven C_f/SiC composite in Run #3. Multiple, periodic, orthogonal cracking of the silicon wafer was observed. This is due the strong brazed bond and CTE mismatch between the silicon wafer and the woven C_f/SiC substrate.

A Comparative Run 3 was performed, in substantially the same manner as Run 3, except the substrate was Si/SiC composite made by reaction bonding, and thus had a CTE of about 2.9 ppm/K, instead of about 1.0 ppm/K for the C_f/SiC composite. These conditions are thus similar to Papenburg's. The silicon reflecting surface did not crack.

In Run #4, a silicon wafer was adhesively bonded to the substrate. The process temperature was less than 100°C. The wafer remained intact, but such a bond is unsatisfactory for a number of reasons, including poor thermal conductivity (heat transfer), poorly matched CTE to silicon and to the substrate, and outgassing, particularly in a vacuum environment such as space. Outgassing in ground-based applications such as semiconductor lithography would be an unacceptable contamination source.

In Run #5, silicon was deposited by a low-temperature CVD process, specifically plasma-enhanced CVD. This process was conducted at about 100°C or below, and yielded a bonded silicon coating in substantially amorphous form. The silicon layer did not crack upon cooling to ambient temperature.

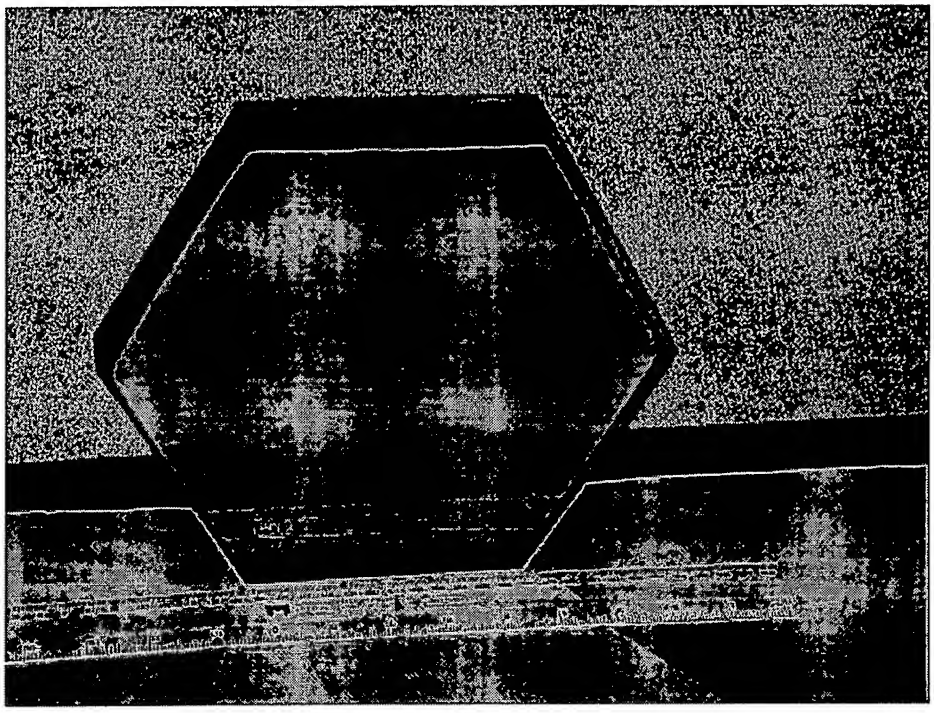

Figure 3. A photo of a finished fiber composite hexagonal mirror (10-inch corner-to-corner) produced using the technique of Run 5.

The following Table summarizes actual and expected results of silicon joining attempts:

Run #	Reflector Material	Substrate	Bond type or process	Process Temperature	Limitations/Problems
1	Silicon/Silicon carbide composite	C_f/SiC	Reaction bonding	1425°C	CTE mismatch-induced stresses are large; →cracking
2	Silicon	C_f/SiC	CVD	1300°C	Same as above
3	Silicon wafer	C_f/SiC	Brazing, e.g., Al-10Si alloy	~600°C	Same as above
Comp-arative 3	Silicon wafer	Si/SiC	Brazing, e.g., Al-10Si alloy	~600°C	No cracking but substrate CTE is too high
4	Silicon wafer	C_f/SiC	Organic glue	<100°C	*Outgassing *Poor heat transfer *CTE mismatch
5	Amorphous silicon	C_f/SiC	PECVD	<100°C	None